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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,941	07/29/2003	Roger A. Fratti	12-19	9094

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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,941	FRATTI ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is FINAL. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 8, and 13 - 16 are rejected as being unpatentable over Hebert (US 6,091,110) in view of Zommer (US 6,162,665), Sergey Savastiouk et al. ("Atmospheric Downstream Plasma," European Semiconductor (June, 1998), pp. 1 – 4).

3. Regarding Claim 1, Hebert discloses a method for controlling the curvature (and stress) (Col.1, lines 54 – 59) of a device (Col. 2, lines 35 – 39), wherein a thin stress compensation layer (24) (Figure 1C) (Col. 2, line 54), is formed on a substrate over the surface of the device.

Additionally, Hebert does not disclose thinning of the substrate or that the overall stress is attributable at least in part to the thinning step. Zommer discloses (Col. 2, lines 8 – 12) that the breakdown voltage is altered by changing the thickness of the substrate to alter resistivity by aggressive backsurface grinding, polishing, or thinning (Col.2, lines 40 – 43). Such techniques, however, are notoriously well known to introduce damage that will alter the residual stress

(See for example, Savastiouk et al., p. 1, para. 4, 6, 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Zommer in Hebert to obtain a backsurface thinned substrate with altered resistivity and breakdown voltage.

4. Regarding Claims 2 and 14, Hebert discloses that the stress compensation layer comprises a thin film (24) (Figure 1C).

5. Regarding Claim 3, Hebert discloses that the power transistor comprises a DMOS device (Col. 2, lines 35 – 36).

6. Regarding Claim 4, Hebert does not disclose that the substrate is thinned by aggressive backside removal procedures. Zommer discloses that the removal is done by backsurface grinding, polishing or thinning. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of Zommer in Hebert to obtain a backsurface "thinned" substrate for improved device properties.

7. Regarding Claims 5 and 6, Hebert discloses that a CVD silicon oxide layer is deposited (Col. 2, lines 54 – 56).

8. Regarding Claim 7, Hebert and Zommer disclose, as discussed for Claim 1, that the thinning of the substrate and application of a stress compensation layer produces a curvature of the device. As such, the "repeated" application would also produce a curvature and is therefore

rejectable using the same criteria.

9. Regarding Claims 8 and 15, Hebert discloses that the thin film serves as an encapulant (Col. 1, lines 54 – 57).

10. Regarding Claims 13 and 16, Hebert discloses a power transistor device (Col. 2, lines 35 – 39), wherein a thin film (24) (Figure 1C), comprising a CVD silicon oxide (Col. 2, line 54), is formed on a substrate as a stress compensation layer. Hebert does not disclose that the deposited oxide stress compensation layer has a tensile stress. However, Sherman discloses (p. 68, 2nd para.) that the stress in the oxide film is tensile, wherein the tensile stress in the oxide film provides "stress relief" in the device (Col. 1, lines 54 – 59). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sherman with Hebert to obtain a film having tensile stress to relieve residual stress within the device.

Additionally, Hebert does not disclose thinning of the substrate. Zommer discloses (Col. 2, lines 8 – 12) that the breakdown voltage is altered by changing the thickness of the substrate to alter resistivity by aggressive backsurface grinding, polishing, or thinning (Col.2, lines 40 – 43). Such techniques, however, are notoriously well known to introduce damage that will alter the residual stress (Savastiouk et al., p. 1, para. 4, 6, 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the procedures of

Zommer in Hebert to obtain a backsurface thinned substrate with altered resistivity and breakdown voltage.

Finally, although Hebert does not explicitly disclose that the device is part of an integrated circuit, it is inherent that the fabrication procedures and intended utilization are part of an integrated circuit manufacturing methodology, wherein the power transistor is incorporated with other elements to produce a working system.

11. Claims 9 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hebert in view of Sherman, Zommer, and Savastiouk et al., as applied to Claims 1 – 8, and 13 – 16, and further in view of Wilson et al. ("Handbook of Multilevel Metallization for Integrated Circuits, Noyes Publ., Westwood, New Jersey, (1993) pp. 223 – 225).

12. Regarding Claims 9 and 10, Hebert does not disclose that the application of the stress compensating layer either maintains or alters the curvature of the device. Wilson et al. disclose that the stress in the structure will cause the wafer to bend (p.223, 2nd para.) and thus alter the curvature according to Equation 13. Hence, the radius of curvature will be inversely proportional to the residual stress and the film thickness, such that, for a given stress, the radius of curvature will either change or remain the same with the application of films of varying thickness. As discussed for Claim 7, optimization can be used to determine the values for thinning and film thickness to either maintain curvature or change curvature. It

would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Hebert to obtain values of the curvature for determining the effectiveness of stress relief.

13. Regarding Claims 11 and 12, Hebert does not disclose a method for monitoring the curvature of the device. Wilson et al. disclose (pp. 223 – 224) that an optical laser system can be utilized to measure curvature using an off-axis technique. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wilson et al. with Hebert to obtain the radius of curvature for power transistor devices.

Response to Arguments

14. Arguments of Applicant with respect to claims have been carefully considered by Examiner, but these have been found to be unpersuasive. Contention of Applicant (p. 2, p.4, Response) that a portion of the stress is not compensated by the stress compensation layer is incorrect. Hebert et al recite (Col. 1, line 55) that the layer is a "stress relief dielectric layer," and residual stress is therefore, compensated. Further, Sherman discloses that dielectric layers prepared in this fashion have "tensile stress."

In regard to statements of Applicant that the combined references do not relate to a compensation of stress or the presence of residual stress in the wafer, Examiner does not concur. Backthinning is known to induce residual stress, as recited in the Sevastiouk et al. reference. Backthinning has been done for a number of years (see for example,Pritchett, US 6,500,764 B1) for reducing thermal effects and resistance (Col. 1, lines 24 – 34). As discussed above, the

"stress relief dielectric layer" will compensate residual stress.

With respect to Hebert and the claim language of Claim 1 (p. 3, Response), it should be noted that the recitation, a method "for controlling curvature of a power transistor" occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

With regard to curvature and stress (p. 3, Response), it is notoriously well known that the deposition of a thin film oxide layer will cause a "bending" or curvature (See for example, Fonash et al., US 6,531,193 B2, Col. 6, lines 50 – 55).

Contentions of Applicant regarding the combination of references (p. 4, Response) have been treated above. Further, the rationale for combining is correct, since it is well known that a higher breakdown voltage is desired for output amplifier devices (See for example, Paul et al., US 6,816,011 B2, Col. 12, lines 57 – 59).

Contrary to contentions of Applicant (p. 5, Response), the combination of references and optimization can be used to maintain curvature. The use of Wilson is valid since it provides a

basis for instrumentally measuring (Eq. 14) the radius of curvature, using optimization to determine film thickness.

References recited herein are provided only to address Arguments of Applicant.

Conclusions

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305 5396.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the

examiner's supervisor, **Eddie Lee**, can be reached on **(703) 308-1690.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee

January 9, 2005